Upgrade of the CDF Track Trigger for High Luminosity Running

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For the XFT Upgrade Group

XFT Requirements

Physics goals

Maintain core high p_T program up to $L=4E32cm^{-2}s^{-1}$

Maintain scenario C two-track trigger to $L=1.5E31cm^{-2}s^{-1}$

- Balances physics goals with realistic operating conditions.
  - Note: extensive simulation work has been done and the upgrade we are pursuing allows us to meet these goals. This was presented at the last Director's Review
  - Here we focus on hardware progress since that review

XFT requirements

Maintain good efficiency (>90%) for high pT tracks.

Improve purity to reduce growth terms

Maintain (or improve) p_T and ϕ_0 resolution

Personnel on XFT II

Baylor University: Dittman, Krumnack

University of Illinois: D.Errede, Junk, Kasten, Levine, Mokos, Pitts, Rogers, Veramendi

Ohio State University: Cochran, Gartner, Hughes, Johnson, Kilminster, Lannon, Olivito, Parks, Winer

Purdue University: Jones

FNAL: S. Holm, T. Shaw, P. Wilson

Documentation

Finder Specification [and schematics]

http://www-ppd.fnal.gov/tshaw.myweb/Stereo_Finder.html

Optical Mezzanine Specification

http://www-ppd.fnal.gov/tshaw.myweb/Xft_upgrade/Mezz_Spec.pdf

Stereo Mezzanine receiver and transition module specfications

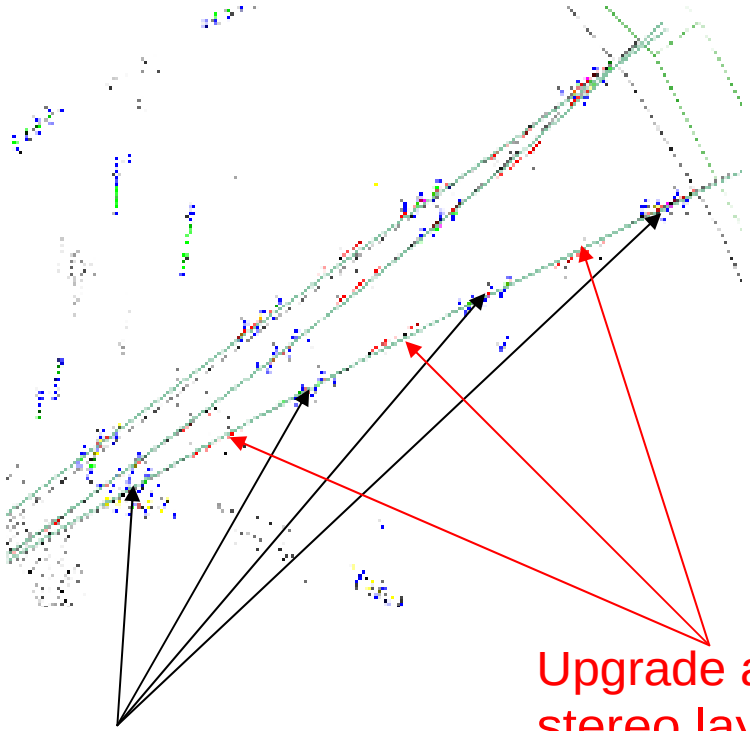
http://www-ppd.fnal.gov/tshaw.myweb/RX_Mezz.html

XFT 2 Simulations (CDF 7039)

SLAM Specification (CDF 7073)

XTC 2 Board (Spec + Implementation) CDF 7360

Upgrading the XFT



Stereo algorithm exploits correlation expected for real tracks

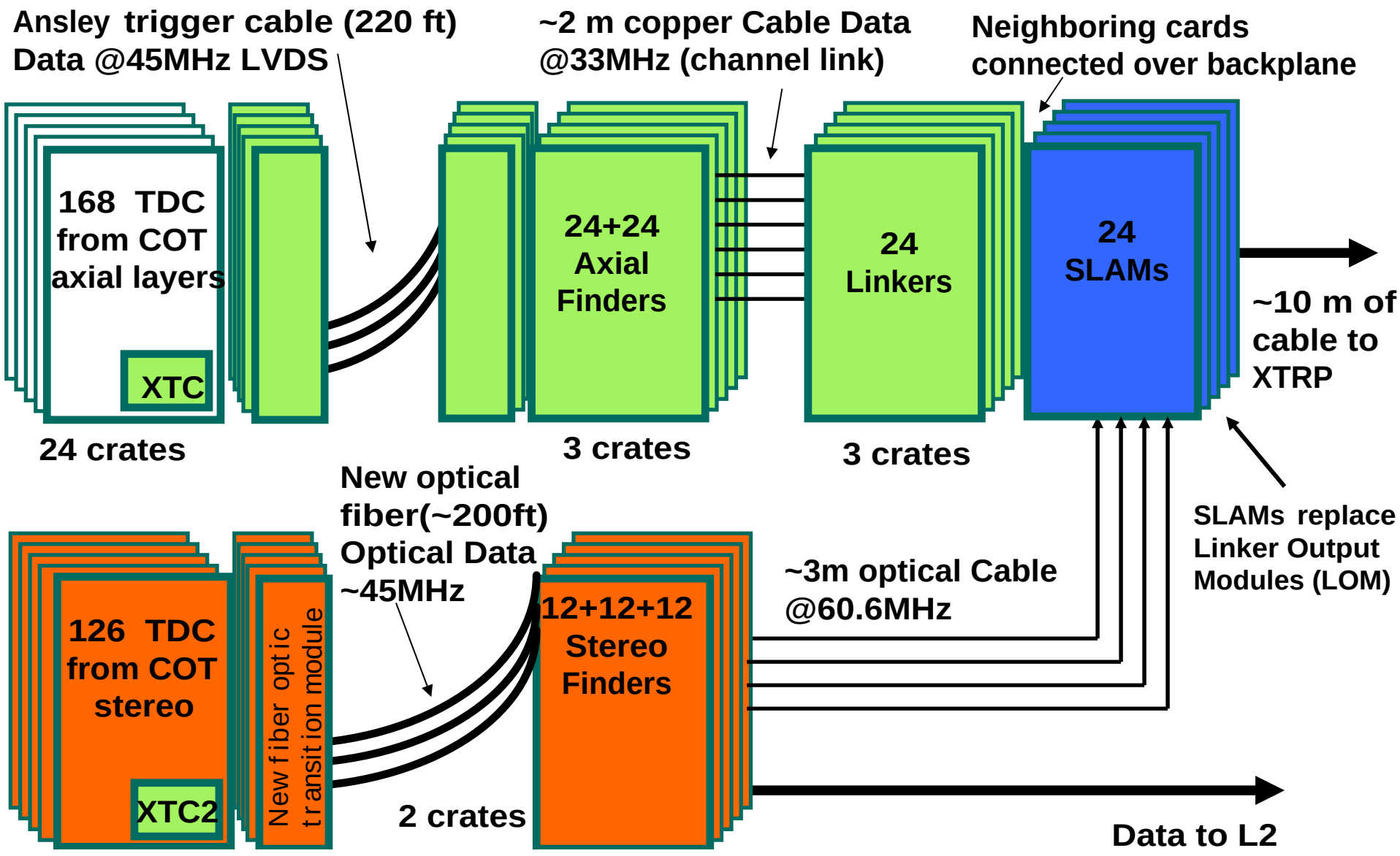
Currrent (Axial) XFT

- **Hit and Segment finding in 4 axial layers; Finder outputs pixels**
- **Linker loops over pixels and search for High Pt tracks; Linker outputs pt and phi in 288 slices**
- **Results reported to XTRP in time for L1 trigger decision**

Upgraded XFT

- **Add hit and segment finding in 3 outer stereo layers; 6 bin timing used for hits; Finder outputs pixels to L1 SLAM and L2**
- **SLAM takes input from axial XFT and Stereo Finders; stereo confirmation bit(s) assigned for all 288 linkers**
- **Results reported to XTRP in time for L1 trigger decision (replaces current axial output)**

XFT Upgrade Configuration



What we are building

TDC mezzanine boards [126 bds]

- Takes COT input data, puts hits into time bins

TDC transition modules [126 bds]

- Holds Tx(transmit) mezzanine board, performs timing & multiplexing

Fiber optic Tx(transmit) and Rx(receiver) mezzanine boards

- Allows for common I/O throughout system.

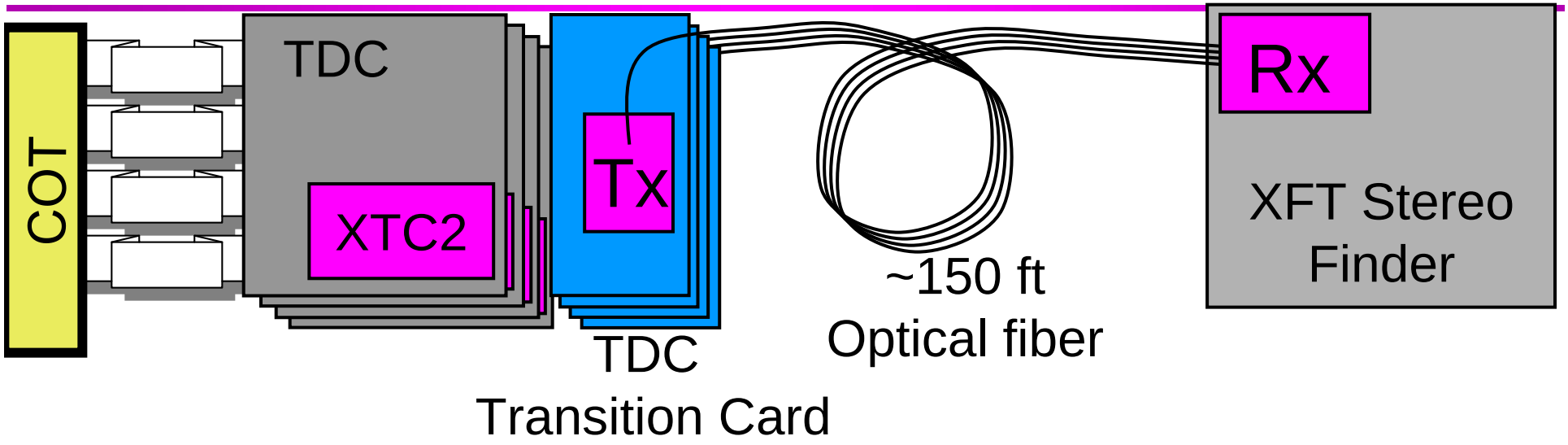
Stereo Finders [3 stereo SL * 12 bd/SL = 36 bds]

- 3x the data (per wire) to process
- Interfaces to L1 SLAM, L2 trigger

Stereo Linker Association Module (SLAM) [24 bds]

- Replaces Linker Output Module
- Merges axial tracks with stereo segments at L1

Getting TDC data to XFT

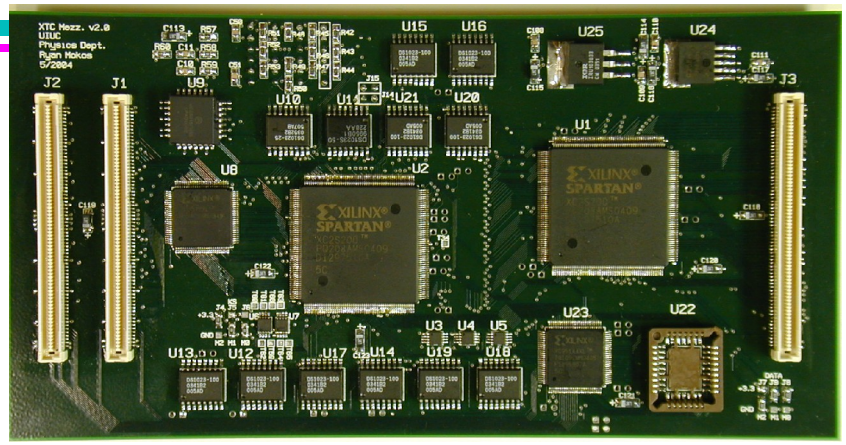


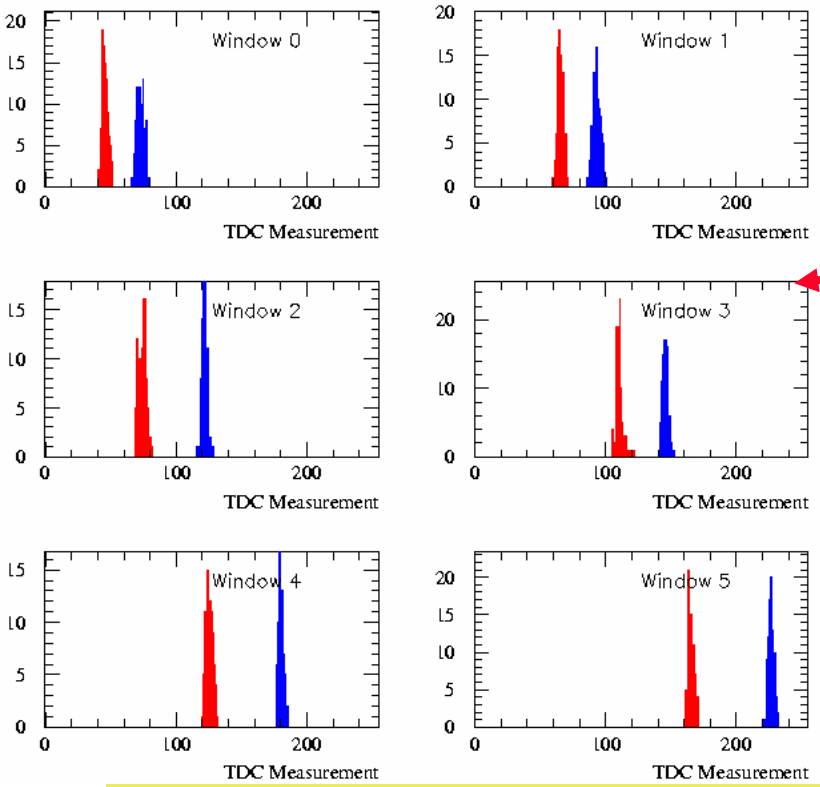
- **COT data split into two paths: trigger and data**
- **Trigger data is put into 6 time bins by the XTC2 mezzanine card**
- **Data driven upstairs to Stereo Finders**
  - **Optical fiber link: Pulsar compatible cards**
  - **Same Tx/Rx technology used in XFT-SLAM and XFT-L2**

XTC2 cards: status

Summer 2004: 10 prototypes made

- Implement timing windows in FPGA
- Full 6 time bin functionality
- Can use a Run 2A (2 bin) mode





Measured start/stop time for each window
Consistent with 3ns timing resolution

Prototype Testing

U of Illinois

- Capture test with Run IIa XFT + Ansleys
- Resolution, stability excellent

Fermilab (WH 14th floor test stand)

- Test with COT front-end system

Fermilab (on CDF detector)

- Installed 4 boards in November 2004
- Successfully read out colliding beam data

Production Order (200 bds) placed Dec 22.

- First assembled boards end of January

XFT Data Path

TDC Transition module

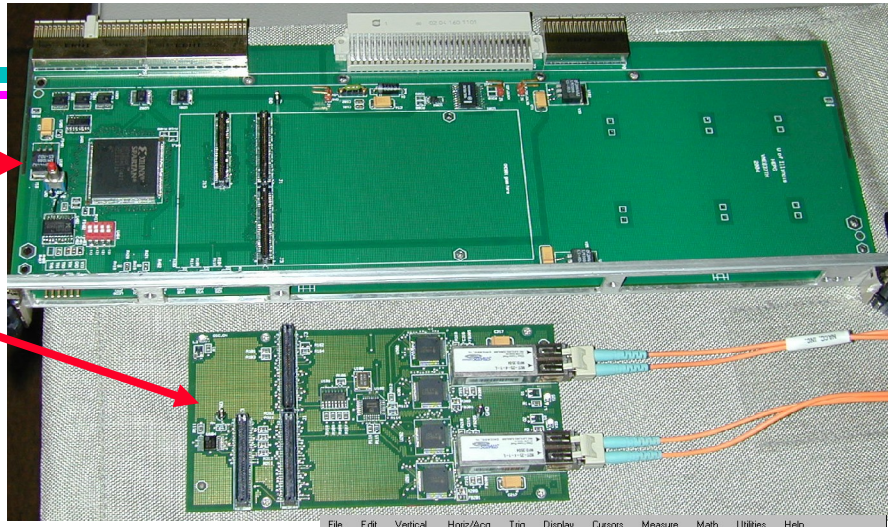
- Timing and multiplexing

Fiber optic transmit board

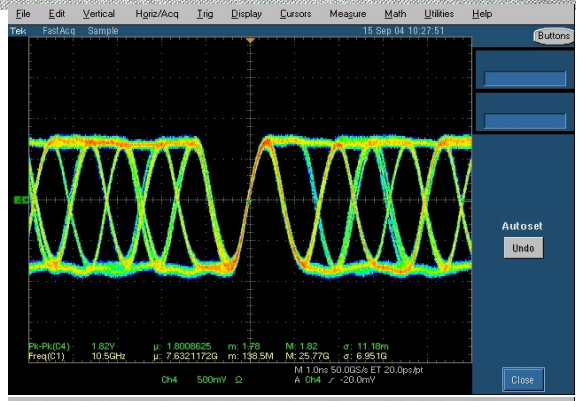
- Use on: TDC TM, SLAM interface

Fiber optic receiver board

- Use on: Finder, L2 Pulsar



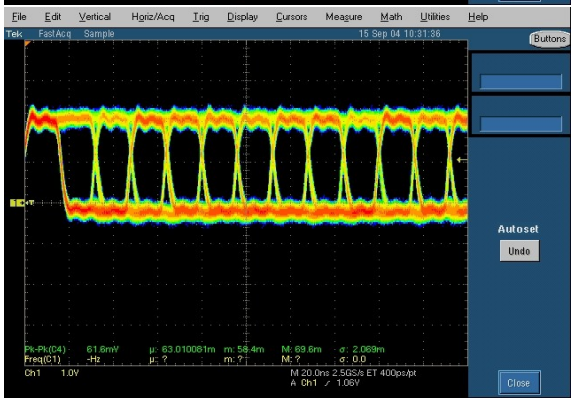
Optical data



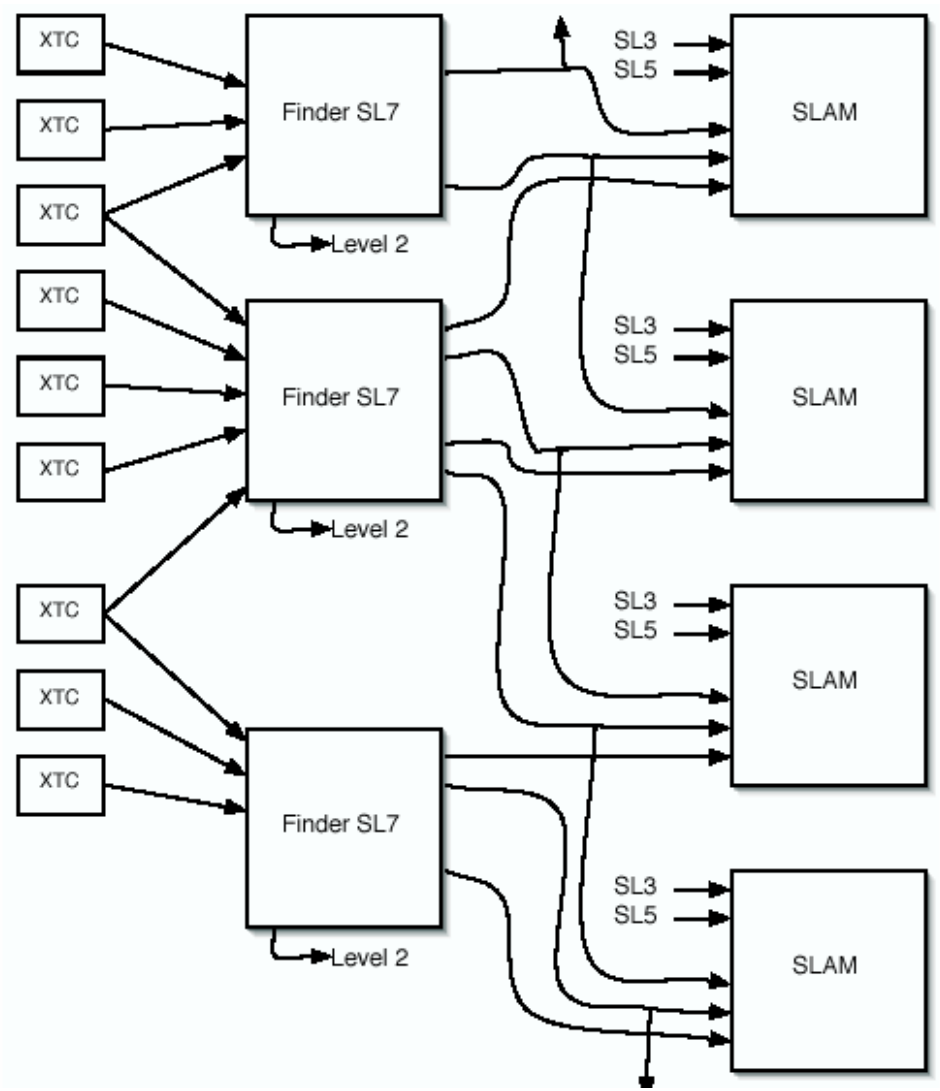
Prototypes built and tested

- Look good.
- Investigating higher data rates
- Production runs will await vertical slice test.

Electrical data



Fibers Used in the XFT Upgrade

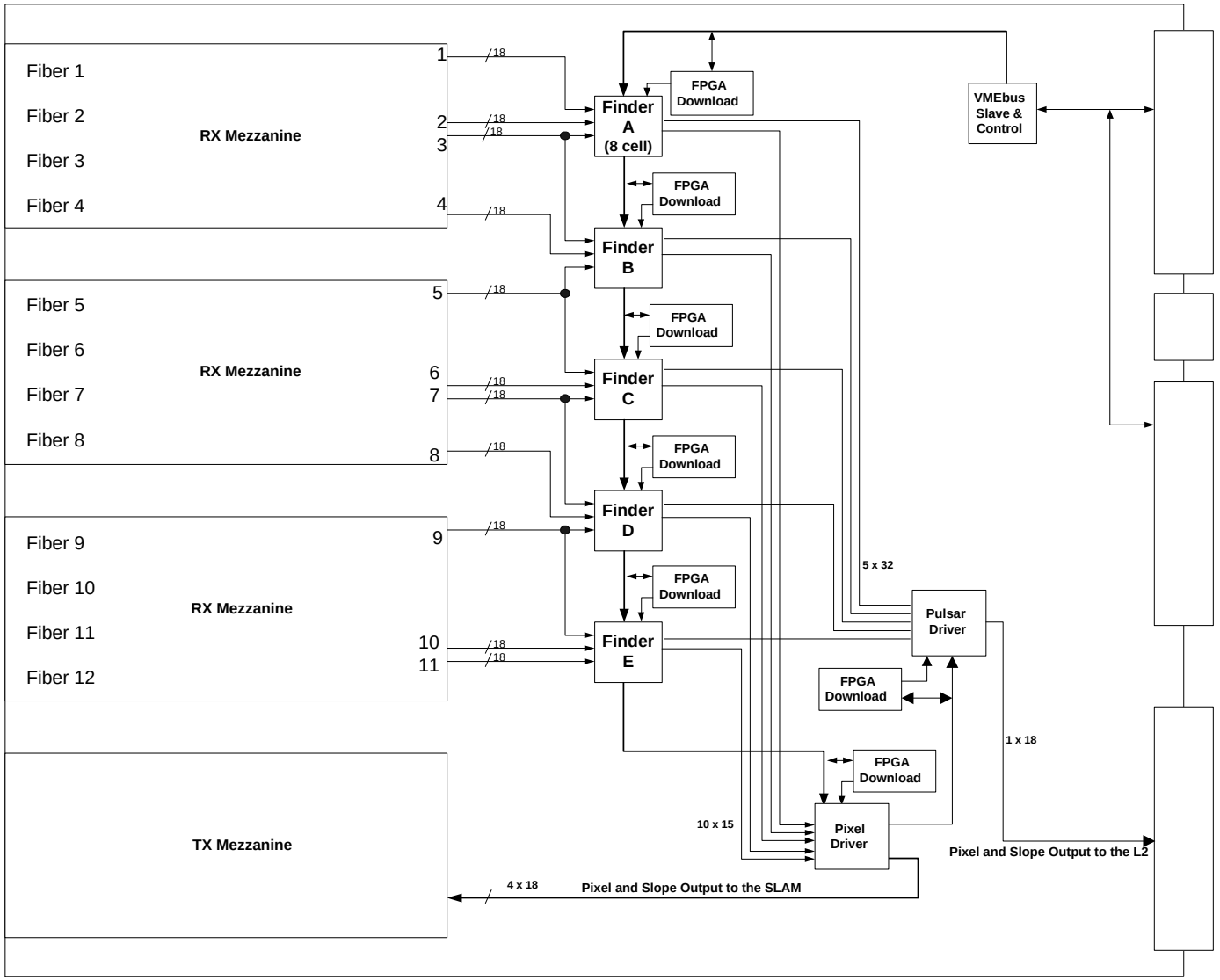


Fibers from XTC to Finder

- 200ft + 2ft breakout each end
- Total installation: 38 bundles of 4 fibers + 36 bundles of 6 fibers
- Pulling fibers expected to take ~7 days

Will need fibers pulled for commissioning transition boards

XFT Stereo Finder Board

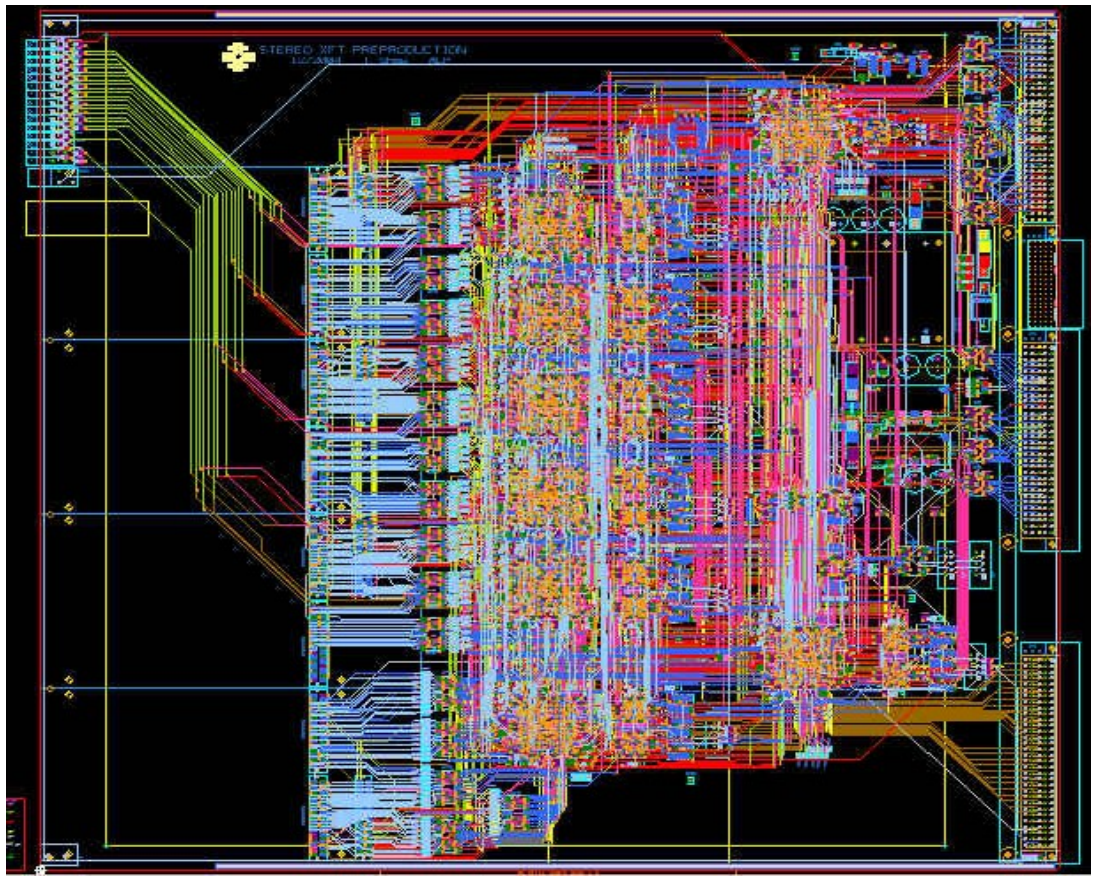


Stereo Finder Board Status

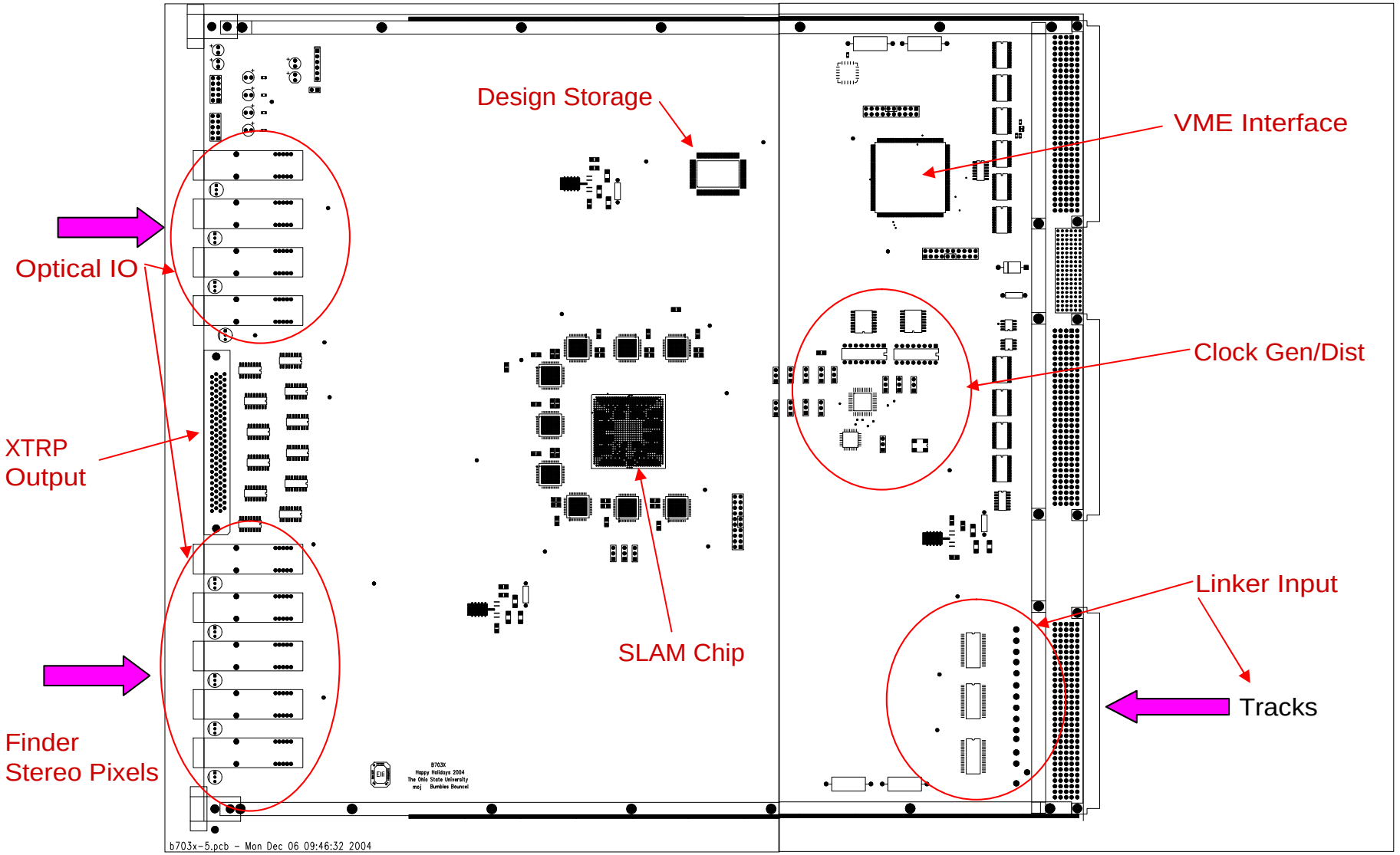
PCB Manufacture/Assembly Job released to Compunetix, Inc. on December 6, 2004

5 boards due back around Jan. 21, 2005

16 layer Board (8 signal/8 planes) – 9Ux400mm format

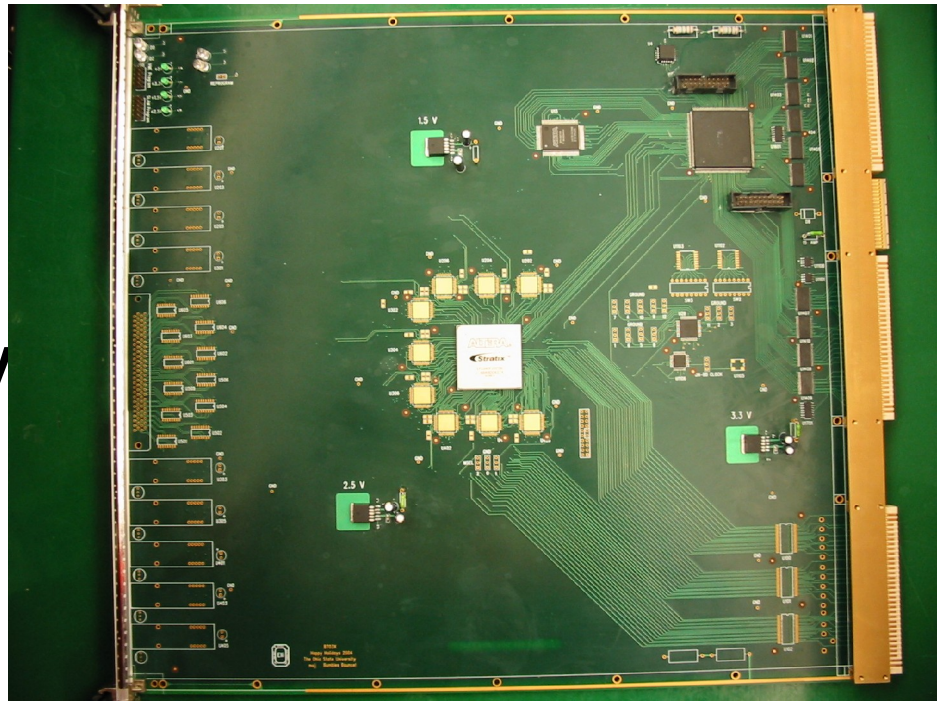


SLAM Board Layout



SLAM Board Status

- **Board received Dec 21, 2004 (Centrix)**
- **Local firm (Dynalab) loaded 1024-pin BGA (SLAM chip)**
- **Remainder of parts stuffed by OSU technicians**
- **Enough parts loaded to test:**
  - **VME interface**
  - **Loading of VME/SLAM chip firmware**
  - **VME/SLAM chip communication**
- **Remainder of parts will be added as needed**
  - **All parts are in hand**



Testing begin this week!

Firmware Progress

The Stereo Finder and SLAM designs make extensive use of reprogrammable devices.

Major progress in firmware over the last 6 months

Functional designs have been implemented

Timing has been studied

Quartus II Version

4.1 Build 181 06/29/2004

SJ Full Version

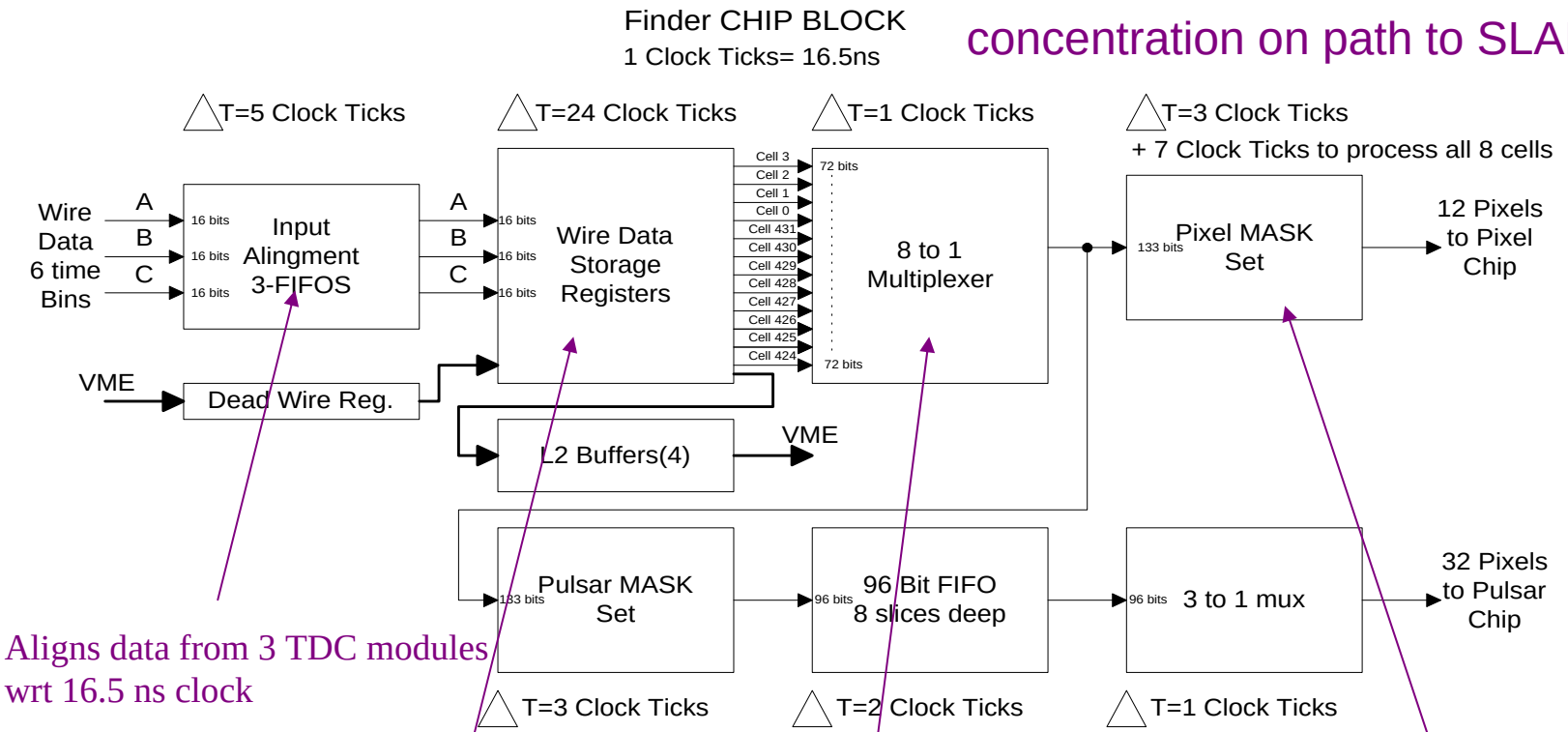
Stereo Chip Compilation

; Family	; Stratix II
; Device	; EP2S60F484C3
; Timing Models	; Preliminary
; Total ALUTs	; 10,602 / 48,352 (21 %)
; Total pins	; 150 / 335 (44 %)
; Total memory bits	; 33,088 / 2,544,192 (1 %)
; DSP block	; 0 / 288 (0 %)
; Total PLLs	; 0 / 6 (0 %)
; Total DLLs	; 0 / 2 (0 %)

SLAM Chip Compilation

; Family	; Stratix
; Device	; EP1S40F1020C5
; Timing Models	; Production
; Total logic elements	; 25,081 / 41,250 (60 %)
; Total pins	; 341 / 782 (43 %)
; Total memory bits	; 6,912 / 3,423,744 (< 1 %)
; DSP block	; 0 / 112 (0 %)
; Total PLLs	; 1 / 12 (8 %)
; Total DLLs	; 0 / 2 (0 %)

Stereo Finder Chip



Aligns data from 3 TDC modules wrt 16.5 ns clock

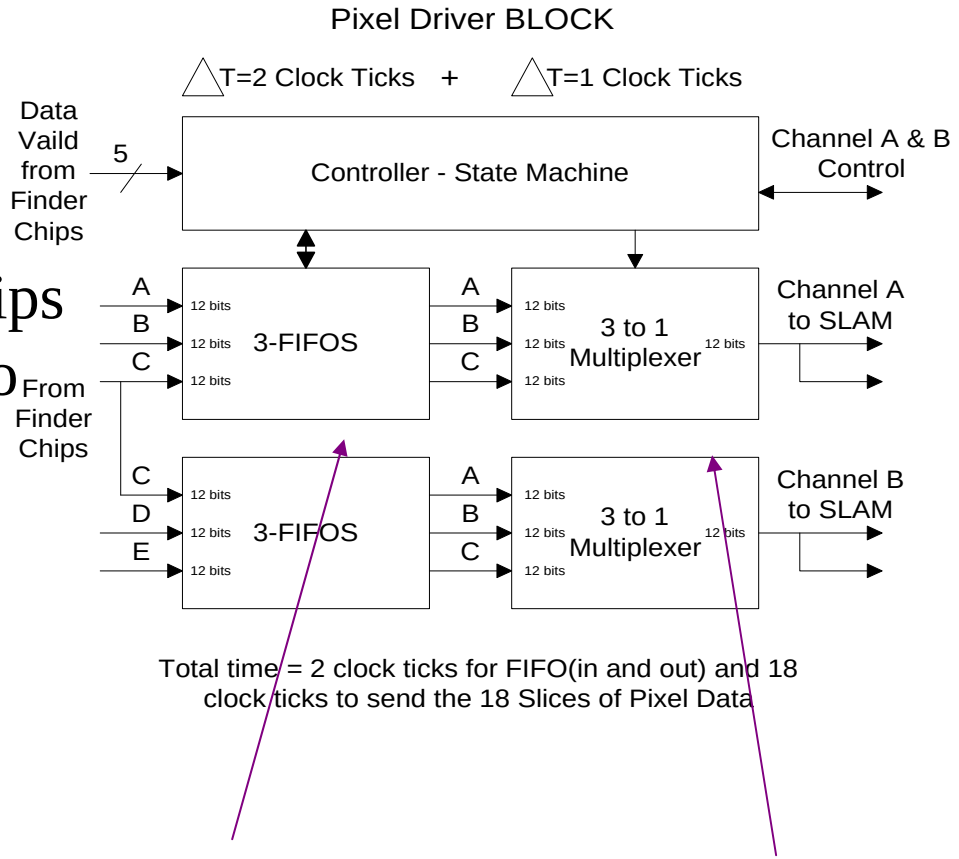
To register 6 time bins for 12 cells, requires 24 time slices

Data multiplexed to provide 133 bits of information for segment finding in one core cell

For each of 8 core cells, finder algorithm is run producing 12 pixels of phi and/or slope output to SLAM module

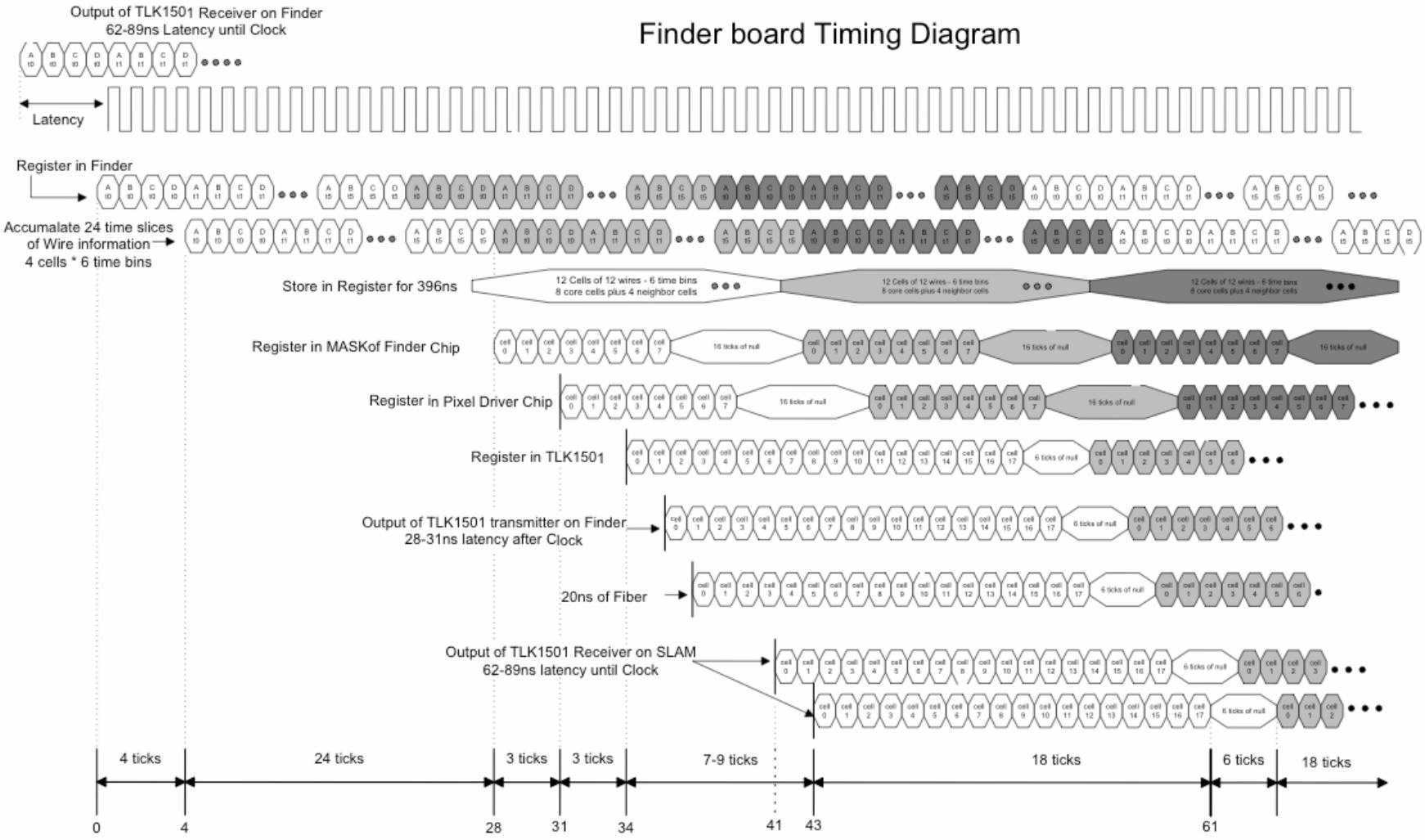
Pixel Driver Chip

Pixels from 5 Finder Chips sent through two paths to SLAM



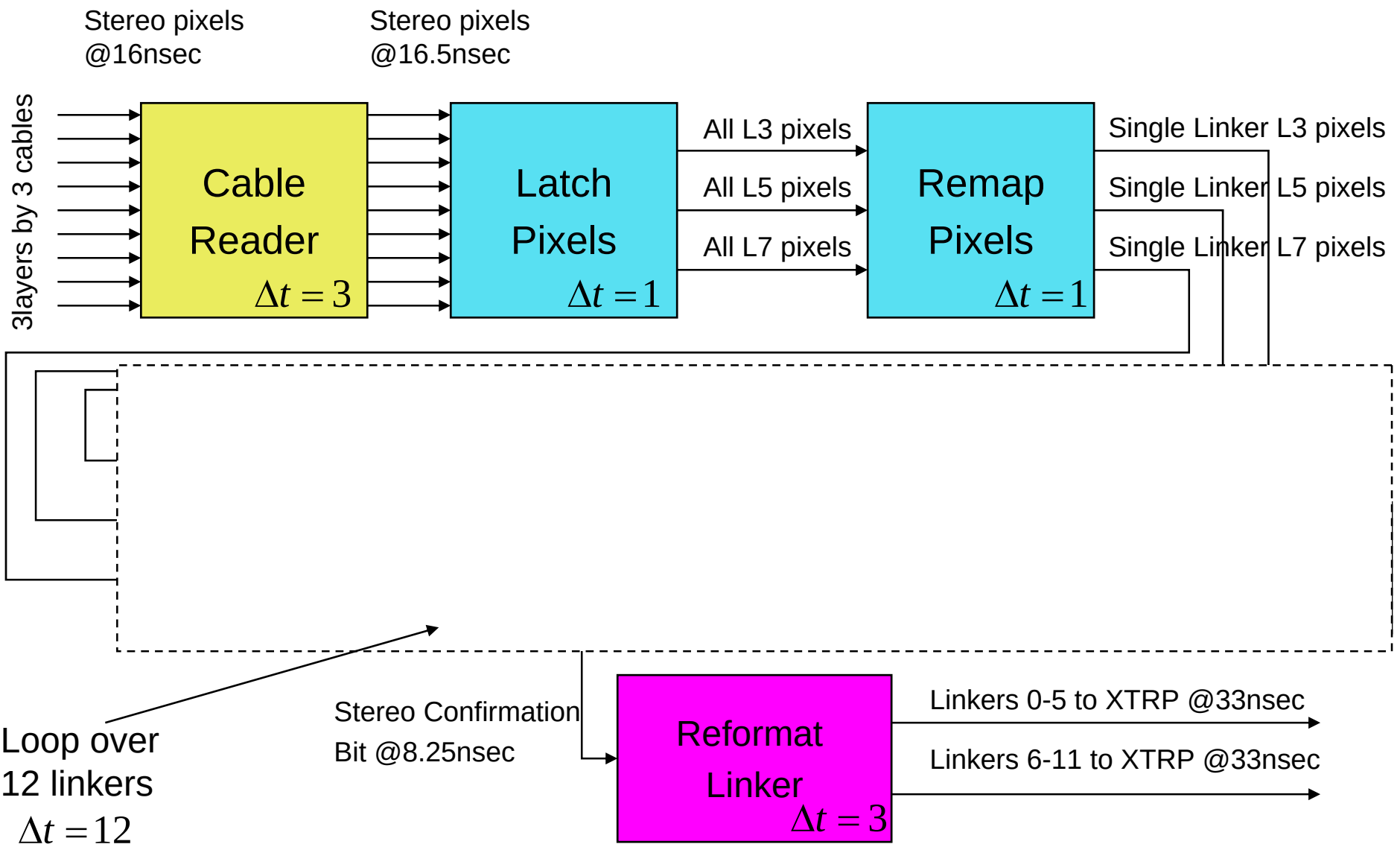
Pixel Data from 3 Finder Chips (18 core cells) are accumulated in each FIFO

Pixel Data sent to SLAM in two 15° slices containing 18 core cells of pixels for association to axial tracks

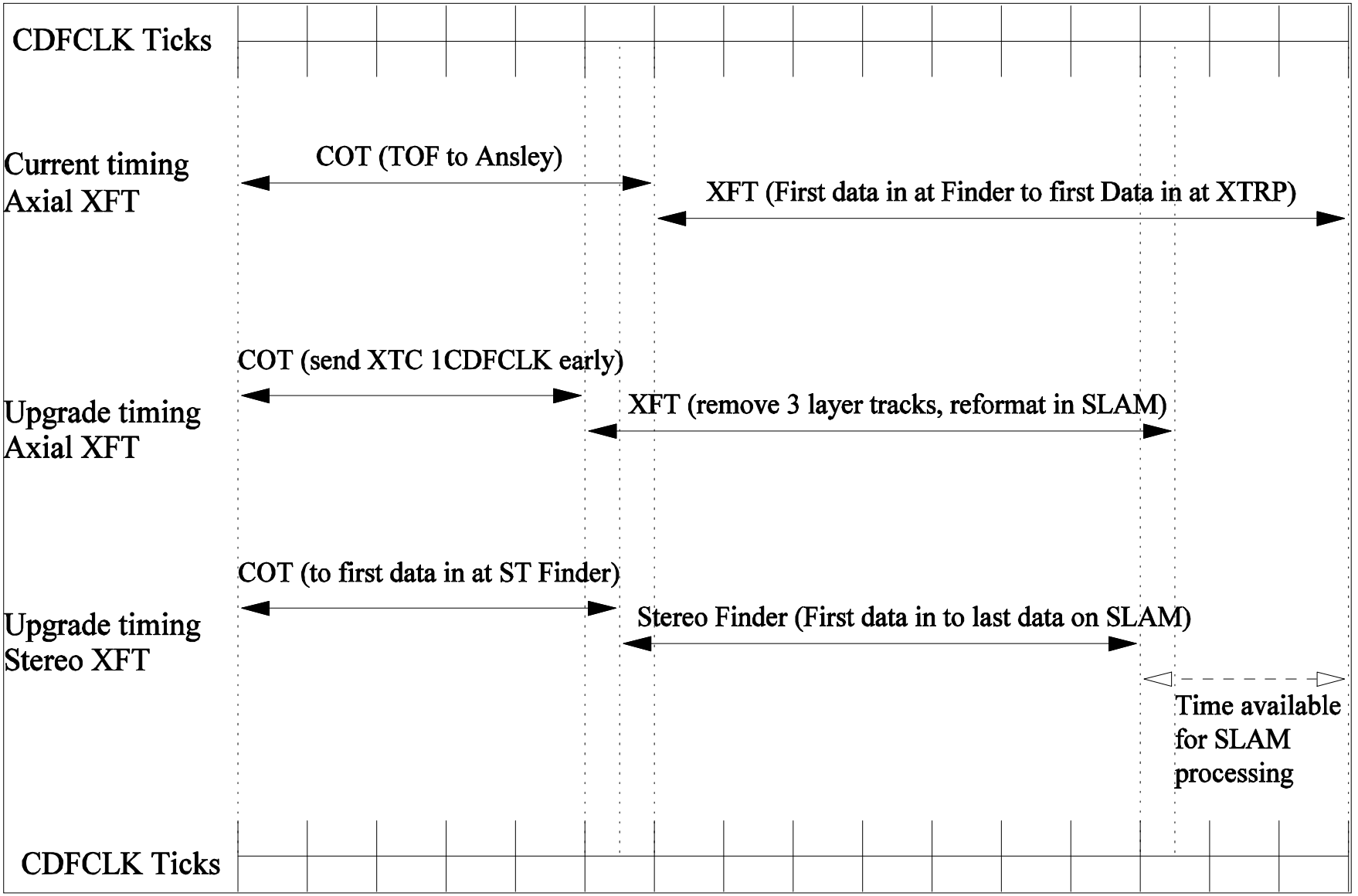


61 (16.5 ns) clock ticks = 1007 ns from when first TDC data arrives to when output of receiver on SLAM has 18 cells

SLAM Chip


Stereo pixels
@16nsec
Stereo pixels
@16.5nsec
3layers by 3 cables
Cable
Reader
$\Delta t = 3$
Latch
Pixels
$\Delta t = 1$
All L3 pixels
All L5 pixels
All L7 pixels
Remap
Pixels
$\Delta t = 1$
Single Linker L3 pixels
Single Linker L5 pixels
Single Linker L7 pixels
Loop over
12 linkers
$\Delta t = 12$
Stereo Confirmation
Bit @8.25nsec
Reformat
Linker
$\Delta t = 3$
Linkers 0-5 to XTRP @33nsec
Linkers 6-11 to XTRP @33nsec

Timing


CDFCLK Ticks
Current timing
Axial XFT
COT (TOF to Ansley)
XFT (First data in at Finder to first Data in at XTRP)
COT (send XTC 1CDFCLK early)
Upgrade timing
Axial XFT
XFT (remove 3 layer tracks, reformat in SLAM)
COT (to first data in at ST Finder)
Upgrade timing
Stereo XFT
Stereo Finder (First data in to last data on SLAM)
Time available
for SLAM
processing
CDFCLK Ticks

Stereo Finder Board Testing

Boards will be individually tested

Initial

- JTAG to check connectivity
- VME slave responses
- FPGA download

Algorithm Tests

- load data in FPGAs, pump through and inspect results

Initial tests will occur at Highrise

Eventually move some testing to CDF

Include SLAM board when ready

SLAM Board Testing

Teststand at OSU is operational:

We are able to run tests with Linker Boards and current Linker Output Module (LOM)

- **Input test vectors driven by and output captured by the Linker Tester Module.**

Initial SLAM Tests: (next 2 weeks)

Basic Tests:

- **VME Interface: reads/writes**
- **Downloading of SLAM Chip.**

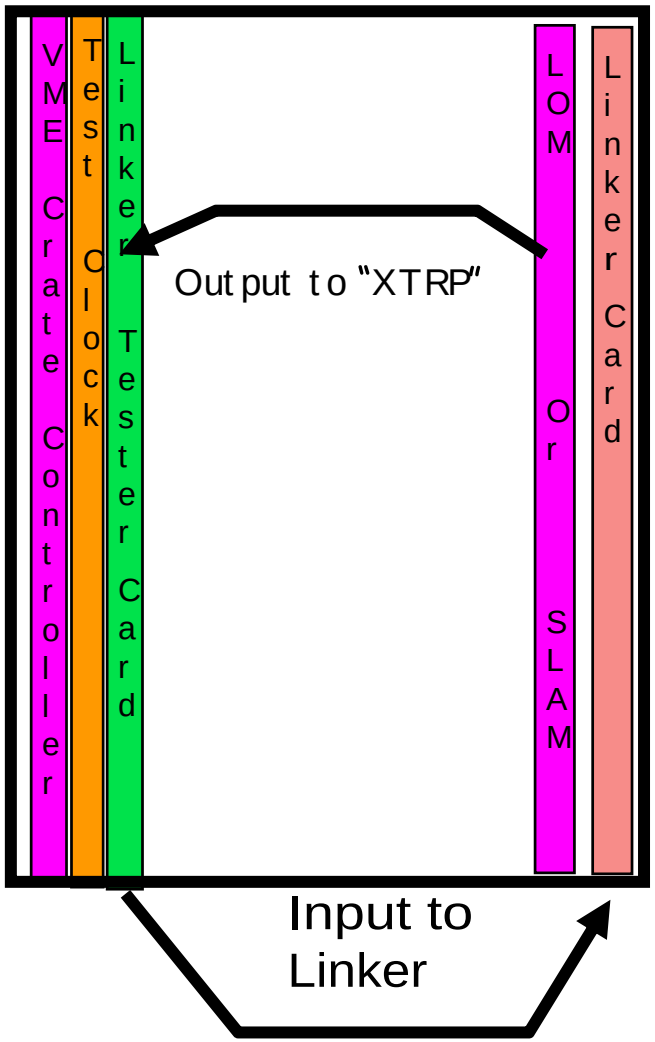
Pass through mode:

- **Can it function as a replacement for the LOM. (Check Timing/Latency)**

Capture Optical Input

- **Drive signals from either the same SLAM or separate SLAM**

Capture Linker Board output



Algorithm Testing

Testing of Full Algorithm (~4-6 Weeks)

XFTSim to generate Input and Output Vectors.

- **Currently do this for Linker**
- **Need to Add Vectors for Stereo Pixels.**
- **Output Vector**
  - **Need to put in bitwise simulation of the SLAM algorithm.**
  - **Output vector will naturally follow.**

Requires Software Development work for XFTSim.

Run at full speed

With testclock issue L1 accepts and L2 Buffers.

- **Determine timing relative to Linker.**

Check Timing with this setup.

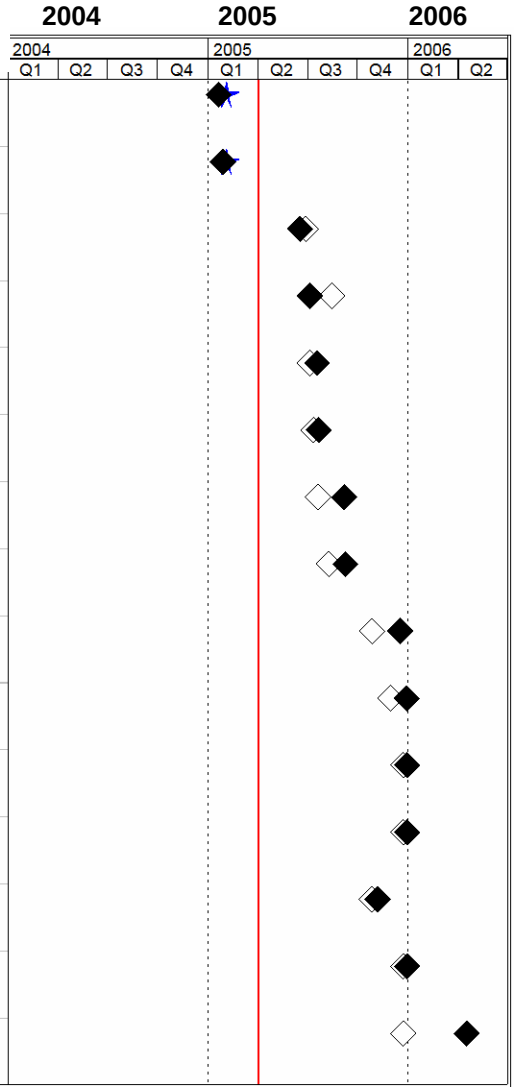
- **Run with modified Linker to speed up timing**
  - **e.g. dropping 3 layer tracks.**
  - **Moving functionality to SLAM from Linker Output Chip.**

Note: Many of the tests will be extensions of existing tests from the Linker Board development. This will require new "cdfvme" code development …but we have a solid foundation to work from.

Can start test with Finder before we are finished with all.

XFT Project Milestones

Name	Forecast	Baseline	Variance
Begin Purchase of Pulsar Board components	11/4/04	10/20/04	2 wks
Begin Production TDC Mezzanine Card	11/3/04	10/28/04	0.8 wks
Receipt of TDC to Finder cables Complete	3/28/05	3/18/05	1.2 wks
Begin Joint Testing with Finder Board	5/16/05	4/4/05	5.8 wks
Begin Production of SLAM Boards	4/4/05	4/18/05	-2 wks
Begin Production TDC Fiber Transition Boards	4/11/05	4/21/05	-1.6 wks
Checkout of TDC Mezzanine Cards Complete	4/20/05	6/6/05	-6.5 wks
Begin Production XFT Finder Boards	5/9/05	6/8/05	-4.2 wks
Checkout of TDC Transition Boards Complete	7/27/05	9/16/05	-7.2 wks
Checkout of SLAM Boards Complete	8/30/05	9/28/05	-4 wks
Finder Board Checkout Complete	9/22/05	9/29/05	-1 wk
XFT Ready for Installation at CDF	9/22/05	9/29/05	-1 wk
Ready for Accelerator Shutdown 2005	7/27/05	8/8/05	-1.4 wks
Finish Run 2b Trigger DAQ project	9/22/05	9/30/05	-1 wk
Data Acquisition and Trigger Upgrades Ready for	9/22/05	1/17/06	-15 wks



◆ Baseline Date
◇ Forecast Date
★ Actual Date

Green milestones are needed before 2005 shutdown

Conclusions

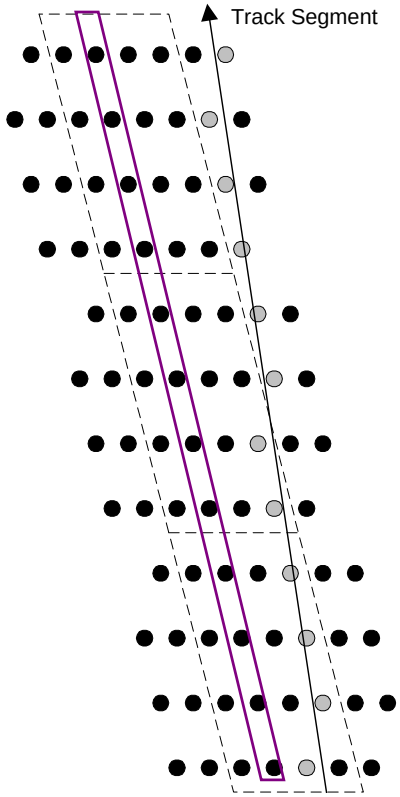
- **Tremendous progress over the past 6 months**
  - **Algorithms finalized**
  - **Prototypes of all boards in hand now or over the next few weeks**
  - **Timing mostly understood**
    - **Still need full verification**
- **Testing of hardware has begun**
  - **XTC2: Production order placed**
  - **SLAM: Pre-production board in hand**
  - **Stereo Finder: Pre-production board expected in ~1week**

Backups

Stereo Finder Algorithm

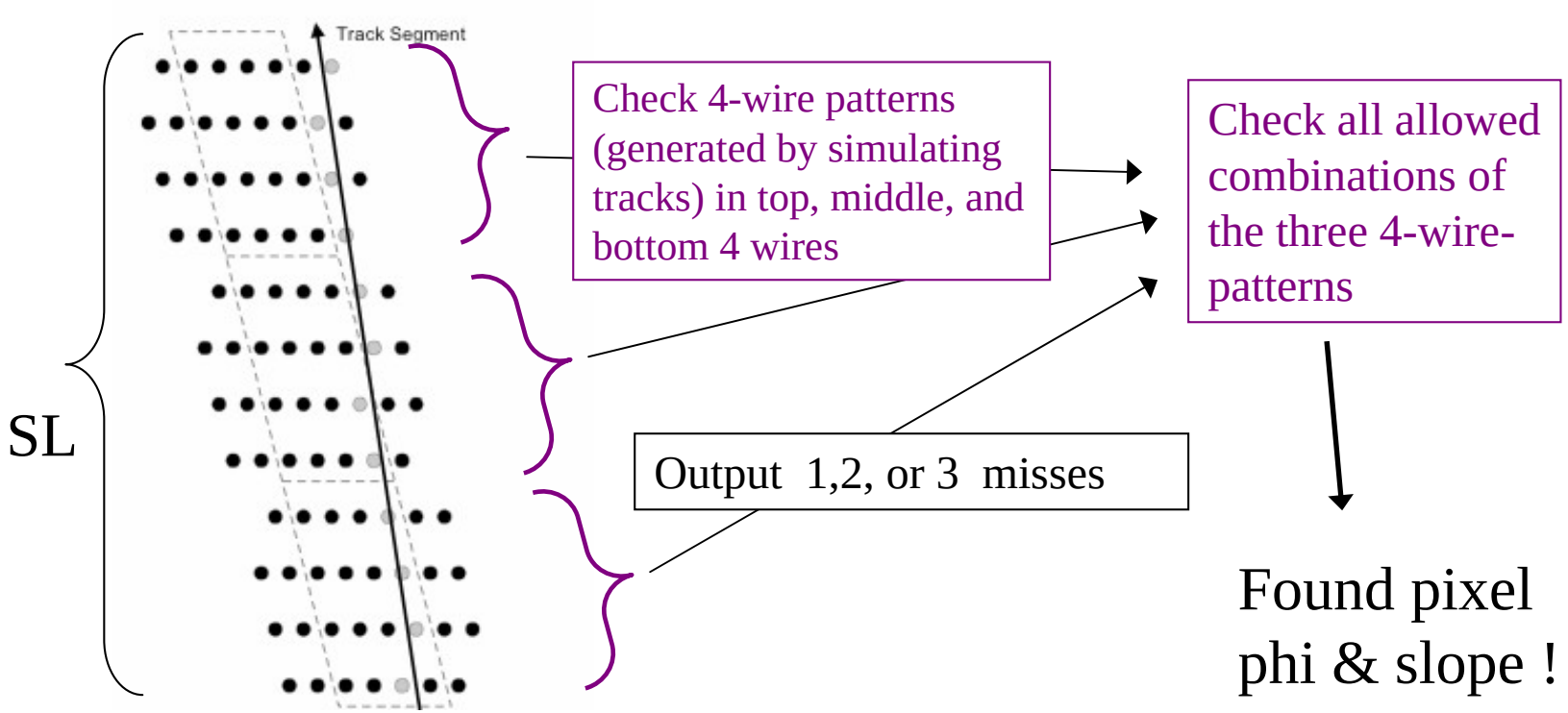
Finder Algorithm

- Similar to axial XFT
- 6 time bins input (72 bits per 12-wire cell) vs 2 time bins(24 bits)
- 8 12-wire cells vs 4 cells per FPGA
- 16.5ns clock vs 33ns clock
- Much larger Mask set
- L2 Pulsar Data(96 bits output)
- Implement in newest ALTERA Stratix 2 FPGA



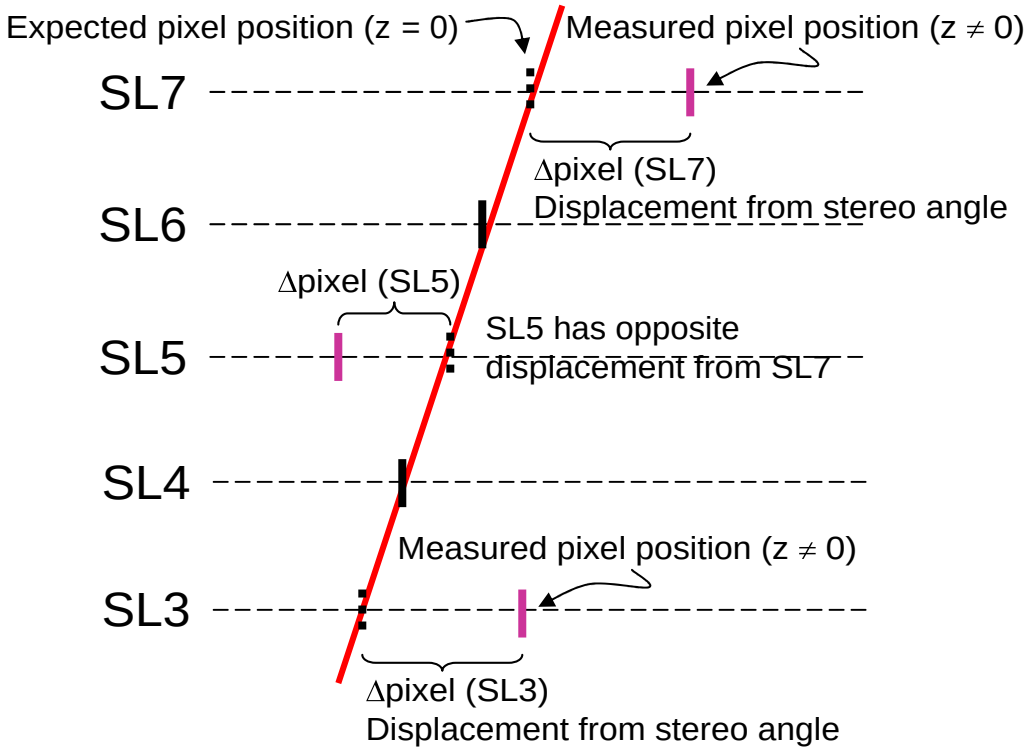
Gray Wires indicate 12 wire mask for the depicted track segment

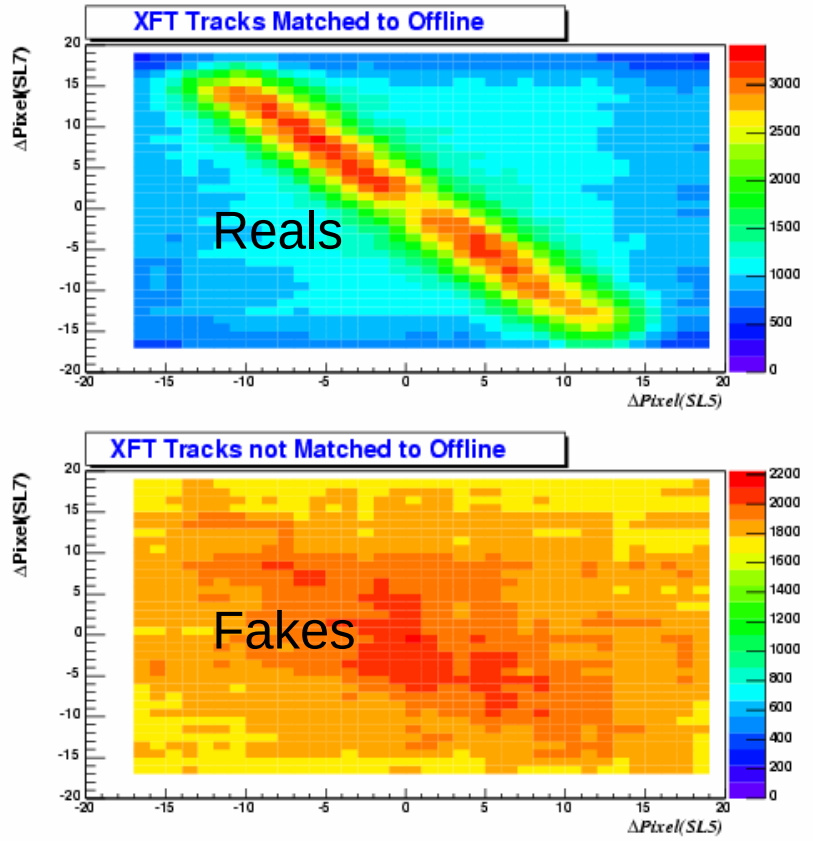
Segment Finding Algorithm



For each SL (3,5,7), there are 3 designs for each allowed number of misses (1,2,or 3)
2 designs can be loaded: one of the above plus a testing algorithm which allows us to input test vectors and verify output through rest of the system

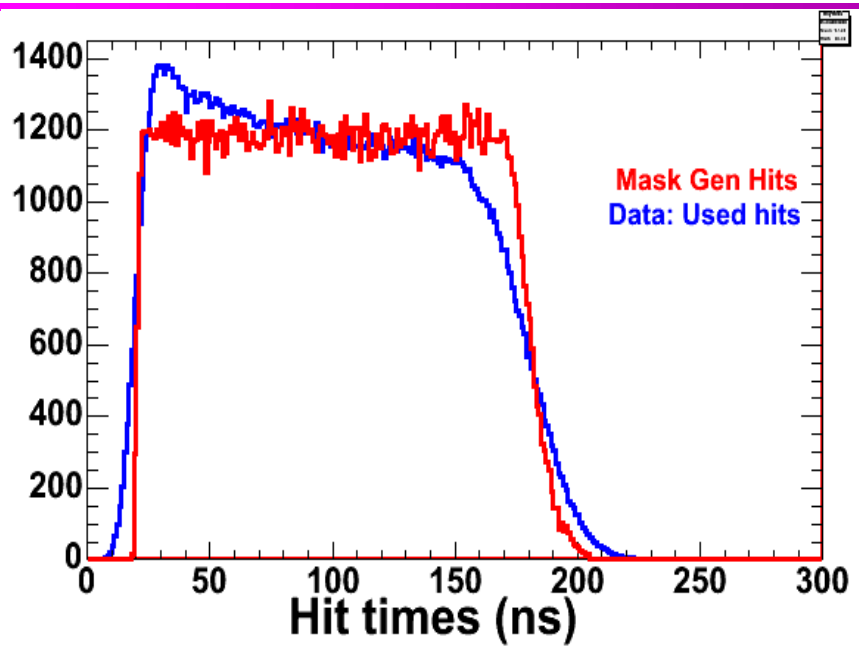
SLAM Algorithm

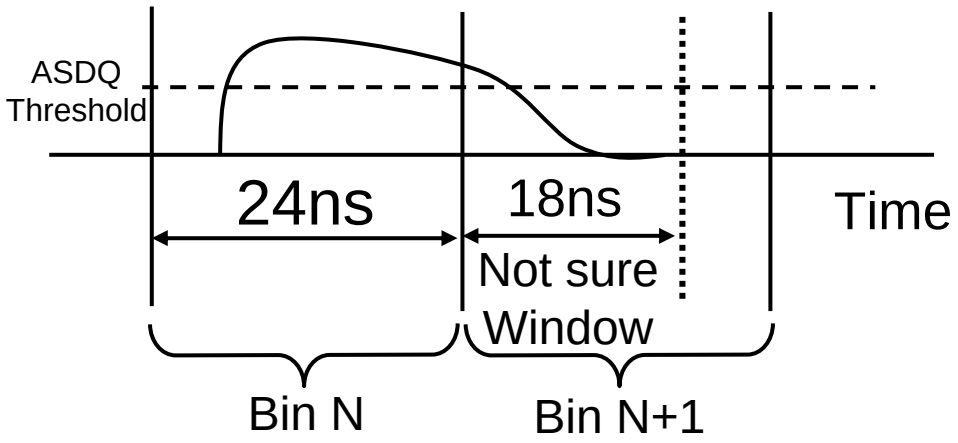




Improving the XTC Algorithm

- **Change binning of hits**
  - **Pattern generation and hit processing had different binning**
  - **Some bins were under-utilized**
  - **Better fake rejection: 20%**
- **"Not sure" window**
  - **Most hits fire two time bins**
  - **<pulse width>~40ns**
  - **Bin width: 24ns**
  - **If hit exists in previous bin, ignore hits at beginning of bin ("not sure window")**
- **Both improvements give an additional ~40% fake rejection over numbers from last XFT review**



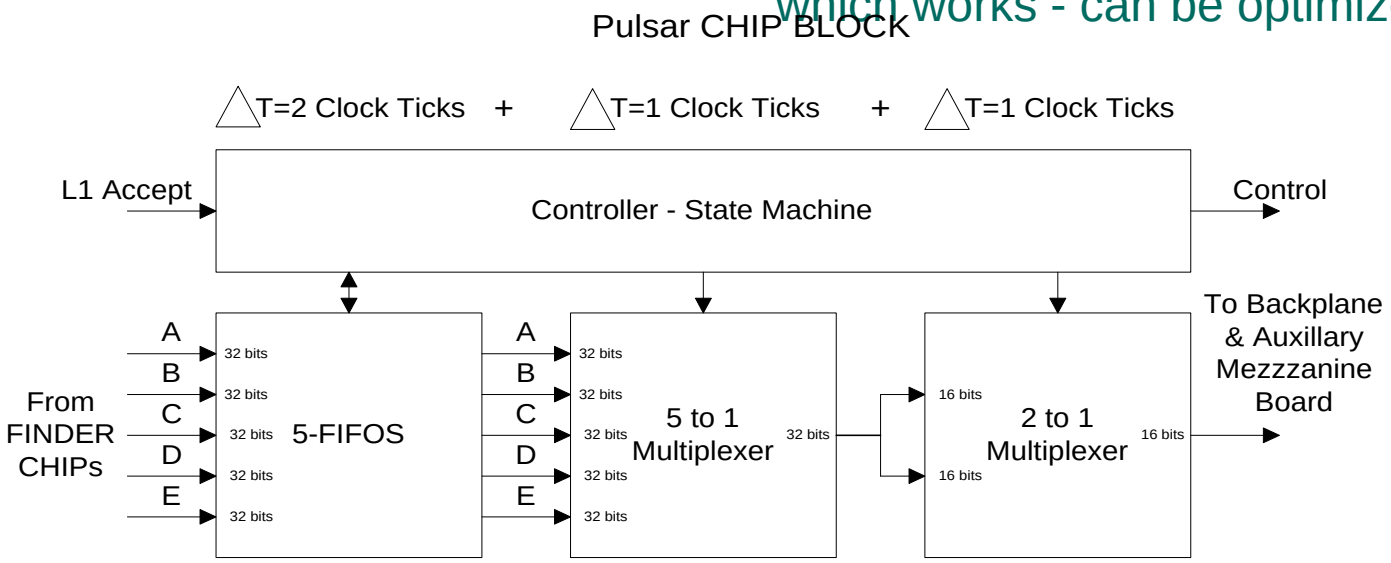


Level 2 Interface

- **"Full" stereo information not available until L2**
  - 3D tracks at L2 used for electrons, muons, ISO, SVT, invariant mass
- **Finder sends segment information to L2 via fiber optic**
  - Using Tx, Rx mezzanine cards (4+1 Pulsars)
- **Data link specified [see Ben's talk]**
  - Segment data: 96 bits per cell=[*e.g.* 12ϕ * 8 slope bits]
  - Maximum bandwidth and data rates well understood.
- **Further details of the L2 implementation are firm/software**
  - Stereo tracking, matching, algorithms
- **L2 portion of the system has received less attention so far.**
- **UC Davis (Robin Erbacher *et al*.) beginning to get involved with this effort.**

L2 Output Chip

demonstration of something
which works - can be optimized

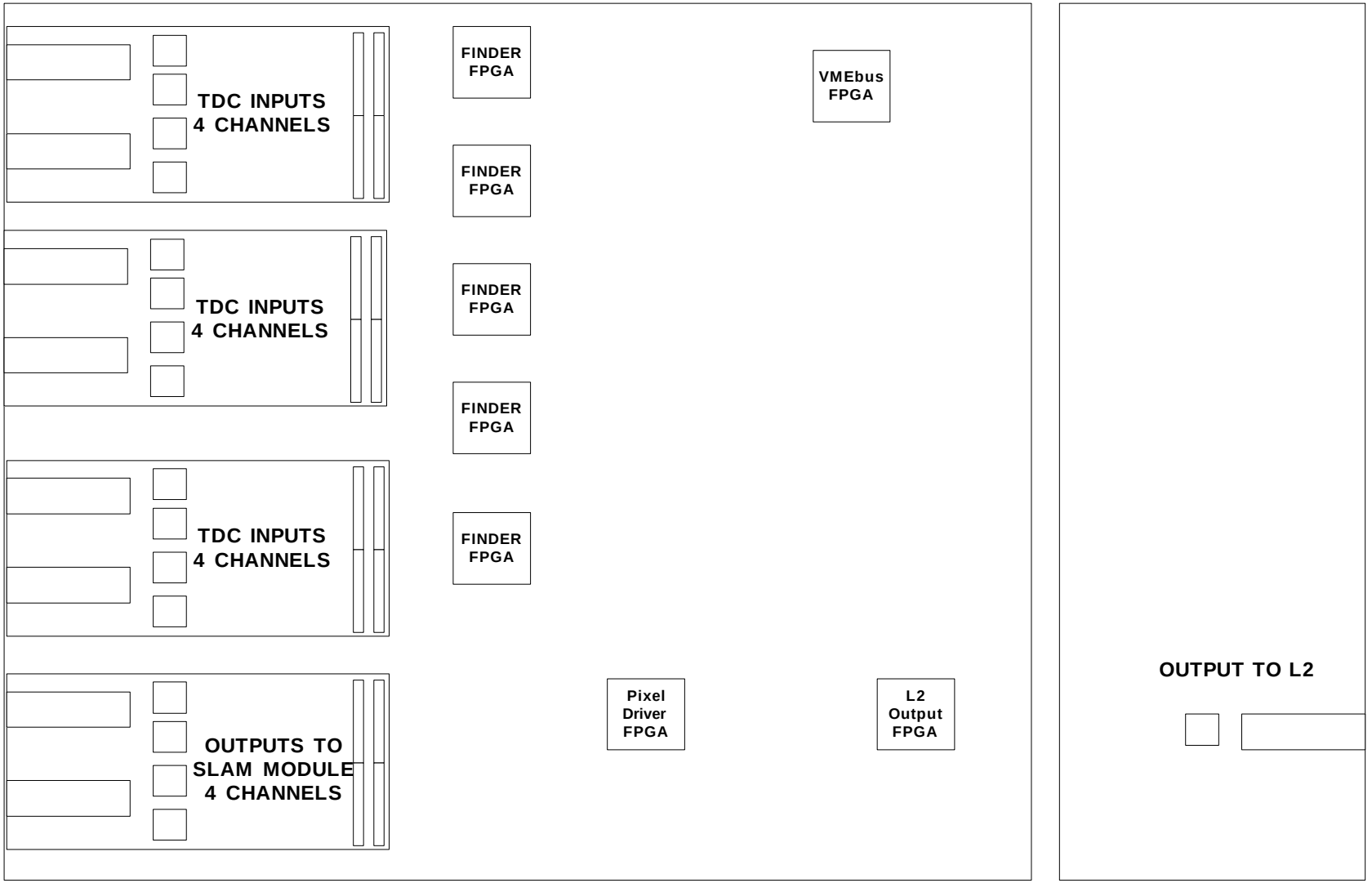


Total time to send data on a L1 Accept = (96 bits/cell * 8 cells/Finder * 4.5 Finders / 16 bits) * 16.5ns = 3.564us

- 32 bits of Pixel data is stored as a slice in the FIFOs, 3 slices per Cell, 8 Cells from each Finder.
- On L1 Accept, FIFO outputs to multiplexers, then sent to PULSAR board. Otherwise, FIFO slice overwritten.

- 96 bits per cell * 8 cells per Finder Chip * 4.5 Finder Chips = 3,456 bits per Finder SL7 board
- 16 bits every 16.5ns, so it will take --> 3,456/16 * 16.5ns = 3.564us

Transition Module – Link to L2



9U x 400mm Main Module

Transition Module

Transition Module

Custom design for Transition Module has been schematically captured

- **2 serial optical links provided off the transition module**
- **each stream will contain identical information**
- **8b/10b encoding utilizing TLK1501 serializer**
- **data stream to be received by the 4 Channel RX_Mezz which is also used on the Stereo XFT main board**

Online Software

- **So far, software developed for testing has been based upon XFT finder-capture tests.**
  - **Most board level testing to utilize software developed for Run 2a**
  - **You will hear a bit about this in other talks.**
- **Plan is to begin utilizing the TDC Test code as the basis for system testing.**
  - **TDC Test uses TRACER test pulse to check TDC performance.**
  - **Utilizes run control code and is well-established code.**
- **Our plan is to append XTC 2 readout [Finder/SLAM/Pulsar] into the TDC Test code.**
  - **Idea is to put pulses in the front end and let the system run in a "normal" mode.**
  - **Will also develop the functionality to put test data in elsewhere.**
- **We are just beginning this transition.**
  - **XTC 2 production check out will be the first place it's heavily used.**
  - **Anticipate this approach playing a major role in integration.**